A MULTI-GIGABIT SIGNAL PROCESSING SYSTEM

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ABSTRACT

Signal processing in the multi-gigabit per second range can be accomplished by making use of a very simple ring diode structure imbedded in a MIC. This circuit can be characterized as a single pole double throw switch with switching times of less than 100 ps. It is capable of performing as the basic element in a variety of processing functions including signal multiplexing, demultiplexing signal sampling and as a shift register. Data rates up to 4 GB/S have been processed using this technique.

I. Introduction

The development of multi-gigabit communication systems requires the application of new design, measurement and analysis techniques as well as the modification of some well-established approaches to microwave circuit design. The multi-gigabit communication system illustrated in Figure 1.1 is illustrative of the range of requirements imposed on the design. In this design it is assumed that the digital data is represented by several Lo data rate channels which are multiplexed and coded to obtain the single serial digital data channel. The reverse operation is required on the receiver end.

The various functional operations required in this system are as follows:

1. First Digital Mux and Second Digital Demux
2. Second Digital Mux
3. Power Amplification
4. First Analog Demux
5. Matched Filter

The three major areas to be emphasized in this paper will be the second digital mux, the first analog demux and the matched filter. The design philosophy for this system is to make maximum use of available components to obtain the desired response characteristics, thus preventing the use of the more advanced devices such as dual gate FET's and Gunn effect logic circuits.

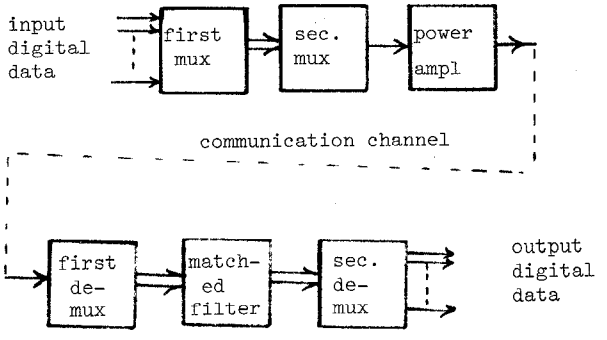

Figure 1.1 Basic Multi-gigabit System

2.1 General Purpose High Speed Logic

The logic operations to be performed by these circuits represent the major portion of the control and data assembly functions as required by the first digital multiplexer in the transmitter and the second digital demultiplexer in the receiver. The actual operating rate for these functions is in the 500 to 1000 MB/S range. The emphasis on the selection of the logic family for performing these rather complex digital operations is to use a standard technique which has sufficient history of successful applications. The chart of Figure 2.1 provides some historical prospective of the status of high speed logic. This chart has been compiled on the basis of the availability of at least three basic logic functions consisting of the 1) flip-flop, 2) gate and 3) exclusive OR. The useful speed is considered equivalent to 1/2 the maximum toggle rate of the flip-flops or the reciprocal of four times the propagation delay. No consideration for power consumption has been given here.

The graph illustrated in Figure 2.1 indicates some impressive speed performance as well as possible advances for the future. However, care must be observed in identifying laboratory and special purpose devices for the general purpose logic elements. In this case, all of the GaAsFET devices identified fall under the classification of laboratory or special purpose devices and, as such, are not suitable for this application at the present time. The general purpose logic family chosen for this task was the 500 MB/S logic family developed by the Motorola Government Electronics Division.

2.2 Special Purpose Very High Speed Logic

The second mux in the transmitter and the first demux in the receiver, as indicated in Figure 1.1, requires a small amount of very high speed logic operations. These logic operations are characterized by 2 to 1 multiplexing and demultiplexing. These logic operations must be performed at the final system rate, but the amount of signal processing is limited to such an extent that special designs can be considered.

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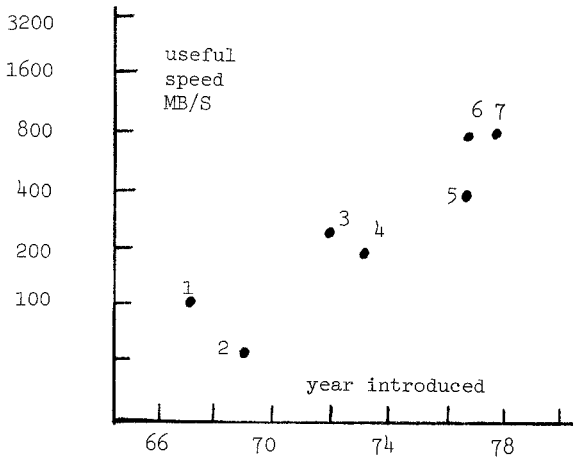


1. Motorola MECL III (BiPolar)
2. Motorola MECL 10000 (BiPolar)
3. Motorola GED High Speed Logic Family (BiPolar)
4. Fairchild 100K (BiPolar)
5. Nippon Electric Logic (BiPolar)
6. Hewlett Packard (GaAsFET)
7. Rockwell International (GaAsFET)

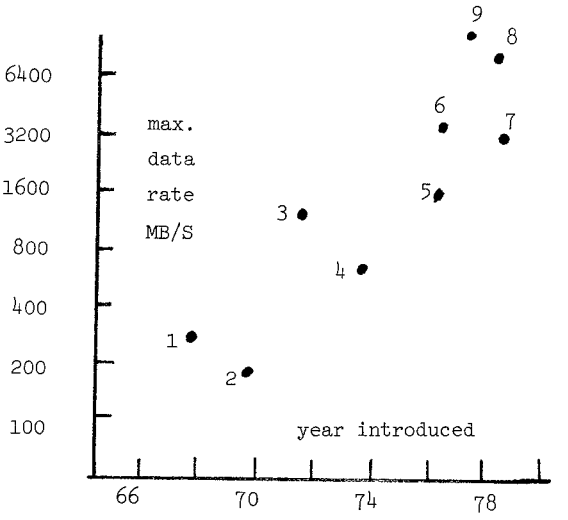
Figure 2.1 General Purpose Logic Speed

The first item of interest is the multiplexer/demultiplexer. The status of multiplexers is very difficult to identify on the basis of pure logic operation. Therefore, assumptions must be made concerning the feasibility of using or modifying an existing component or design. The graph illustrated in Figure 2.2 identifies the maximum data rate capability of various forms of components suitable for multiplexing and demultiplexing. Obviously all of the devices indicated on Figure 2.1 are suitable for this application. However, the maximum rate is greater since the complexity is less.

The timing accuracy obtainable from the multiplexing operation is related to the reciprocal of the bandwidth capability. In the case of the VARI-L DBM-1800, the RF bandwidth is approximately 22 GHz and the IF bandwidth is 7 GHz. This extreme bandwidth and the corresponding balance of approximately 20 dB implies a timing accuracy of better than 10 picoseconds.

It should be noted here that minor modifications of the double balanced mixer configuration will result in a 2 to 1 multiplexer or 1 to 2 demultiplexer.

Gunn effect and other more exotic logic circuits have not been considered here because of the questionable availability of the devices.



1. thru 7 same as Figure 2.1
8. VARI-L Double Balanced Mixer DBM-1800
9. RHG Electronics Lab DBMH 2-18

Figure 2.2 Special Purpose Logic Speed

3.1 High Speed Multiplexing

The basic approach for this system is to make use of a diode switching arrangement which can be characterized as a single pole double throw switch. This circuit makes use of a Schottky diode ring configuration and connected in the basic circuit illustrated in Figure 3.1.

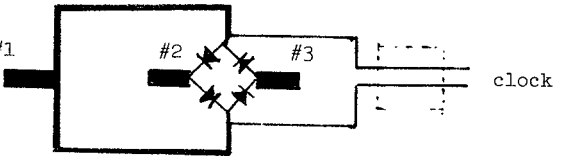


Figure 3.1 Basic Diode Switch

The circuit arrangement has been configured such that it will work as a multiplexer or demultiplexer. The length of the 100 ohm balanced loop is sufficient to offer a high impedance to the clock frequency. The clock is fed to the diodes with a balanced transmission line and has a large common mode inductance in order to minimize the low frequency signal loss. Five to ten mw of clock power is required to operate the swtich and the nominal signal levels are .3 to .5 volts with approximately 2 dB signal loss encountered in the switching operation. Switching times of less than 100 ps can be easily achieved and clock fed thru of approximately 10% of the nominal output has been observed.

3.2 Multiplexer Operation

Operation of the swtich as a 4 to 1 multiplexer is illustrated in Figure 3.2. This circuit has been designed for four channels of 500 MB/S input digital data input to obtain a single 2 GB/S data channel. Figure 3.3 and 3.4 illustrate the output at one GB/S

and 2 GB/S. Figure 3.5 illustrates the response of a 2 to 1 multiplexer operating at 4 GB/S output.

3.3 Demultiplexer Operation

The demultiplexer design has been configured in this system such that it is the first signal processing operation performed in the system. Therefore, input impedance and noise figure are important in this design. Figure 3.6 illustrates the circuit arrangement used for the 2 to 1 demux. Good impedance match is obtained by placing the amplifier at 1/4 wave length from the switching diodes. This procedure results in a reflection coefficient equal to the square of the amplifier reflection coefficient. The noise figure is approximately equal to the amplifier noise figure plus the diode switch loss.

A measured noise figure of approximately 3 dB was obtained for this demultiplexer operating at 2 GB/S. The reflection coefficient was less than 10% for a 100 ps input rise time signal.

3.4 Matched Filter

The matched filter can be implemented at various points within the system depending on the amount of demultiplexing used. Three basic requirements are imposed on the matched filter 1) linear filtering to maximize the signal to noise ratio at a particular sampling time, 2) sampling the signal at the optimum time, and 3) threshold decision. The first operation, that of linear filtering, is achieved by designing the amplifiers with the proper frequency response characteristics. The third operation is achieved by a limiting amplifier followed by a clocked flip-flop.

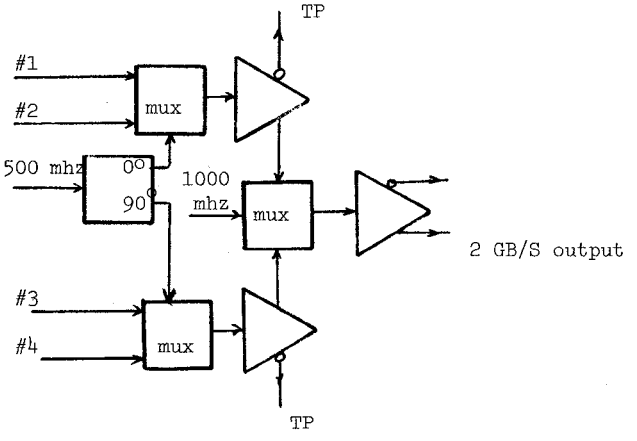


Figure 3.2 4 to 1 Multiplexer

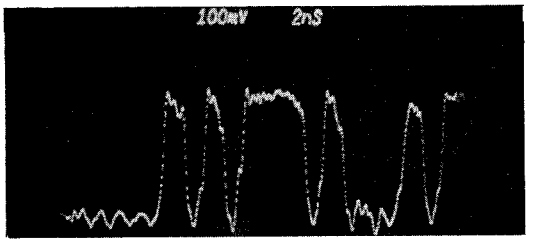


Figure 3.3 1 GB/S Mux Output

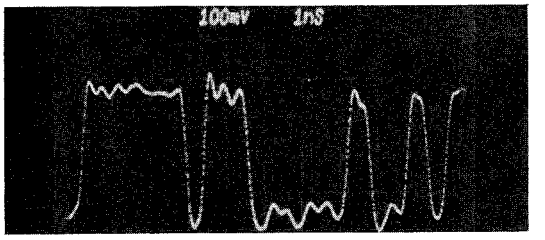


Figure 3.4 2 GB/S Mux Output

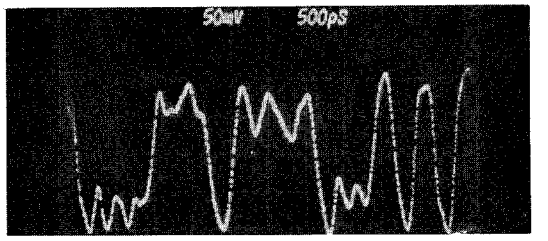


Figure 3.5 4 GB/S Mux Output

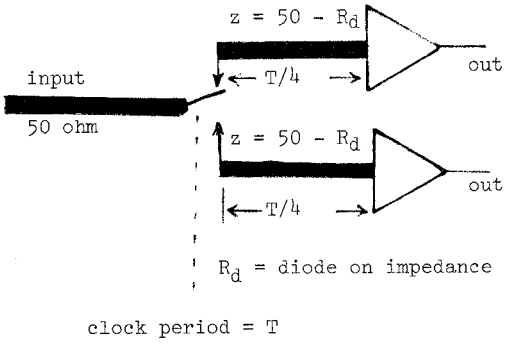


Figure 3.6

The sampling operation must be performed within a very narrow time window, typically less than 10% of the bit period. In this system the sampling is accomplished on the 1000 MB/S channel using the diode switch in a configuration illustrated in Figure 3.7.

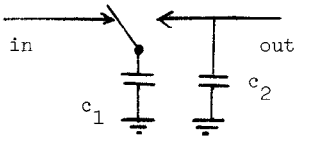


Figure 3.7 Sampling Gate

This circuit is configured such that the swtich allows C_1 to be charged to the input signal voltage and then a portion of this charge is transferred to C_2 ($C_2 \ll C_1$) when the clock changes the switch position. This provides for a sampling window of less than 100 ps. It should be observed that this circuit is the analog equivalent of master/slave flip-flop since the output and input are never simultaneously connected. At the present time a design for a multi-gigabit shift register using this basic concept is in the evaluation process.

4.1 Conclusion

Detailed performance of the completed multi-gigabit processing system have not been completely evaluated as of paper deadline. However, the unit has been assembled and preliminary evaluations indicate that performances within 2 dB of the theoretical will be obtained for 2 GB/S operation. The use of diode type of switches for several general purpose signal processing functions at the multi-gigabit per second rate can be achieved, and can provide significant performance improvement in high data rate systems which require hardware implementation with today's technology.